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EXAMINER

CHEN, TSE W

ART UNIT PAPER NUMBER

2116

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/814,321

Applicant(s)

FEIERBACH, GARY F.

Examiner

Tse Chen

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14, 16-26 and 28-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14, 16-26 and 28-39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

RD

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated May 2, 2005.

2. Claims 1-14, 16-26, and 28-39 are presented for examination. Applicant has canceled claims 15 and 27.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley, U.S. Patent 6219796, in view of Fletcher et al., U.S. Patent 6611920, hereinafter Fletcher.

5. In re claim 1, Bartley discloses a method for operating a microprocessor [10] to reduce power consumption [abstract], the microprocessor including a functional unit [11] formed of a plurality of stages [functional units] [col.3, ll.1-30, ll.41-65], the method comprising:

- Evaluating instructions to be executed to determine the operation type of each of said instructions, the instructions to be executed depending on operation type by said plurality of stages of said functional unit [col.4, ll.54-57; col.5, ll.1-15, ll.33-44, ll.51-57].
- Producing activity indicators [bit level machine code of either sleep or active implicit restoration instructions] by reading an operation type from an instruction and providing an associated signal [bit level machine code of either sleep or active implicit restoration

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instructions] based upon the operation types of said instructions [col.4, ll.54-57; col.5, ll.1-2, ll.33-44, ll.51-57; col.6, ll.8-18].

- Following said steps of evaluating said instructions and producing said activity indicators, controlling the supply of current to each of said plurality of stages such that only selected stages of said plurality of stages will draw current from a power supply, the controlling being based upon activity indicators associated with each of said stages [col.6, ll.33-52; powering down is done after evaluating and producing steps].
- Advancing said instructions with the microprocessor [col.3, ll.16-30; operations advanced serially in stages].
- Executing said instructions that are within each of said selected stages [col.3, ll.52-61].

6. Bartley did not disclose explicitly that the stages are arranged in series or discuss the details of controlling the supply of current.

7. Fletcher discloses a method for operating a microprocessor [integrated circuit] to reduce power consumption [abstract], the microprocessor including a functional unit [FUB logic 310] formed of a plurality of stages [logical stages 310.1-310.N], where said stages of said functional unit are arranged in series [pipeline], the method comprising:

- Producing activity indicators [enable, disable] by reading an operation type from an instruction [instruction itself indicates operation type to determine enabling/disabling of clock] and providing an associated signal comprising one of a clock marker [enable] or a no-clock marker [disable] based upon the operation types of said instructions [col.3, ll.53-67].

- Following a step of producing activity indicators, controlling the supply of current to each of said plurality of stages by providing a clock signal [primary clock] and the activity indicators to a logic gate [330] that determines that only selected stages of said plurality of stages will draw current from a power supply, the controlling being based upon activity indicators associated with each of said stages [col.3, ll.53-67; col.4, ll.1-14, ll.27-30; clock and activity indicators from scheduler control current draw following the production of activity indicators].
- Advancing the instructions within said microprocessor [col.3, ll.53-67; col.4, l.61 -- col.5, l.5].
- Executing said instructions that are within each of said selected stages [col.4, ll.27-37].

8. It would have been obvious to one of ordinary skill in the art, having the teachings of Bartley and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Bartley to include the functional unit as taught by Fletcher, in order to obtain the functional unit having the plurality of independently controlled stages arranged in series, as the pipeline series arrangement of stages is a very well known arrangement suitable for use with the microprocessor of Bartley; and providing the associated signal comprising one of a clock marker or a no-clock marker based upon the operation types of the instructions, as the utilization of clock to control the supply of current is a very well known concept suitable for use with the microprocessor of Bartley. One of ordinary skill in the art would have been motivated to make such a combination as it increases processing efficiency [via pipeline arrangement] and provides a refined way [via clock control] to decrease power consumption in a processor as the processing power increases and potential overheating is a problem [Fletcher: col.1, ll.13-32].

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9. As to claim 2, Bartley discloses the microprocessor that is a very long instruction word processor [col.3, ll.41-44].
10. As to claim 3, Bartley discloses the evaluating operates to determine whether each of said instructions is an operation instruction type [active] or a no-operation instruction type [sleep] [col.5, l.51 - col.6, l.7].
11. As to claim 4, Fletcher discloses the type of instructions executed in each of said selected stages is an operation instruction type [col.4, ll.27-60].
12. As to claim 5, Bartley discloses the producing operates to produce a power-on activity indicator associated with operation instruction types [implicit], and a power-off activity indicator associated with no-operation instruction types [explicit] [col.5, l.51 - col.6, l.18].
13. As to claim 6, Fletcher discloses the selected stages are associated with power-on activity indicators, and wherein the remaining stages are associated with power-off activity indicators [col.4, l.61 -- col.5, l.13].
14. As to claim 7, Fletcher discloses the controlling operation further comprises transmitting a clock signal only to the selected stages of the functional unit [col.4, ll.10-14].
15. As to claim 8, Fletcher discloses the method further comprising repeating all of the steps for successive instructions [fig.3; pipeline architecture repeats for all instructions].
16. Claims 9-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley in view of Fletcher and Matter et al., U.S. Patent 5392437, hereinafter Matter.
17. In re claim 9, Bartley discloses a method for operating a microprocessor [10] to reduce power consumption [abstract], the microprocessor including a functional unit [11] formed of a plurality of stages [functional units] [col.3, ll.1-30, ll.41-65], the method comprising:

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- Receiving instructions at an instruction evaluation unit [dispatch and decode units 11b and 11c] [inherently, instructions have to be received in order to be dispatched and decoded or evaluated].
- Evaluating instructions by said instruction evaluation unit to determine the operation type contained within said instructions, the instructions to be executed depending on operation type by said plurality of stages of said functional unit [col.4, ll.54-57; col.5, ll.1-15, ll.33-44, ll.51-57].
- Controlling the supply of current to each of said plurality of stages such that only selected stages of said plurality of stages will draw current from a power supply, the controlling being based upon activity indicators associated with each of said stages [col.6, ll.33-52; powering down is done after evaluating and producing steps].
- Advancing said instructions with the microprocessor [col.3, ll.16-30; operations advanced serially in stages].
- Executing said instructions that are within each of said selected stages [col.3, ll.52-61].

18. Bartley did not discuss details relating to the stages or an instruction register.

19. In regards to the stages, Fletcher discloses a method for operating a microprocessor [integrated circuit] to reduce power consumption [abstract], the microprocessor including a functional unit [FUB logic 310] formed of a plurality of stages [logical stages 310.1-310.N], where said stages of said functional unit are arranged in series [pipeline], the method comprising:

- Receiving instructions at an instruction evaluation unit [scheduler] [col.3, ll.53-67].
- Transmitting a null-bit [deactivated valid signal] from said instruction evaluation unit to a shift register memory device [340] [col.4, ll.17-19] when said instructions contain a no-

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operation instruction [col.3, ll.23-25, ll.53-67; col.4, ll.48-53; in the broadest interpretation, a no-operation instruction instructs the scheduler to disable power to the particular functional unit], and transmitting a 1-bit [Vcc active level valid signal] from said instruction evaluation unit to said memory device when said instructions contain an operation instruction [col.4, ll.27-32], each of said null-bit and 1-bit being associated with a particular stage of said functional unit [col.4, l.27 -- col.5, l.13].

- Controlling the supply of current to each of said plurality of stages such that said stages of said functional unit associated with a 1-bit draw current and said stages of said functional unit associated with a null-bit do not draw current [col.4, ll.1-14; clock and enable valid signal controls current draw].
- Advancing said instructions within said microprocessor [col.4, l.61 -- col.5, l.5].
- Executing said instructions that are within each of said stages that is associated with a 1-bit [col.4, ll.27-37].

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Bartley and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Bartley to include the functional unit as taught by Fletcher, in order to obtain the functional unit having the plurality of independently controlled stages arranged in series, as the pipeline series arrangement of stages is a very well known arrangement suitable for use with the microprocessor of Bartley. One of ordinary skill in the art would have been motivated to make such a combination as it increases processing efficiency [via pipeline arrangement] and provides a refined way to decrease power consumption in a processor as the processing power increases and potential overheating is a problem [Fletcher: col.1, ll.13-32].

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21. In regards to an instruction register, Matter discloses a method for operating a microprocessor [100] to reduce power consumption [abstract], the method comprising:

- Receiving instructions at an instruction evaluation unit [decoder and microcode units 102 and 103] from an instruction register [cache 101], which temporarily stores a specific instruction before execution [col.5, ll.39-40].

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Matter and Bartley before him at the time the invention was made, to modify the microprocessor as taught by Matter to include the instruction register as taught by Fletcher, in order to obtain the microprocessor with an instruction register. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well-known suitable way to store a specific instruction before execution.

23. As to claim 10, Bartley discloses the microprocessor that is a very long instruction word processor [col.3, ll.41-44].

24. As to claim 11, Fletcher disclosed the controlling operation further comprises: transmitting a clock signal to only said stages associated with a 1-bit, such that the stages associated with a null-bit do not receive a clock signal [col.4, ll.10-14].

25. As to claim 12, Fletcher discloses the method further comprising transmitting a clock signal to the memory device, the clock signal to each of said stages being transmitted after the signal to said memory device is transmitted [col.4, ll.6-47].

26. As to claim 13, Fletcher discloses the microprocessor contains a plurality of memory devices and a plurality of functional units, each of said functional units being connected to a respective one of said plurality of memory device [fig.1; col.2, ll.25-34].

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27. As to claim 14, Bartley discloses the microprocessor is a very long instruction word processor, each instruction containing a plurality of sub-instructions, each of said sub-instructions assigned to one or more of the plurality of functional units [col.3, ll.41-44].

28. As to claim 16, Fletcher discloses the method further comprising repeating all of the steps for successive instructions [fig.3; pipeline architecture repeats for all instructions].

29. Claims 17-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matter in view of Fletcher and Sproch et al., U.S. Patent 6247134, hereinafter Sproch.

30. In re claim 17, Matter discloses a microprocessor [100] that operates in a manner that conserves power [abstract], comprising:

- An instruction register [cache 101] for temporarily storing a next instruction to be executed [col.5, ll.39-40; prefetches next instruction to be executed].
- An instruction evaluation unit [decoder 102 and microcode unit 103] that is connected to said instruction register such that said instruction evaluation unit receives said next instruction from said instruction register, said instruction evaluation unit being configured to evaluate said next instruction [col.5, ll.36-49].
- A functional unit [integer and floating point execution units 104 and 105] for executing instructions [col.5, ll.46-53].

31. Matter did not discuss details of the units or a stage activation controller.

32. Fletcher discloses a microprocessor [integrated circuit] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- An instruction evaluation unit [scheduler] being configured to evaluate a next instruction in order to produce activity indicators [valid signal for enabling and deactivated valid

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signal for disabling] by reading an operation type from the instruction and providing an associated signal comprising one of a clock marker [Vcc active level valid signal] or a no-clock marker [deactivated valid signal] based upon the operation types of said instructions [col.3, ll.23-25, ll.53-67; col.4, l.27 - col.5, l.13].

- A functional unit [FUB logic 310] for executing instructions [col.3, ll.58-67], said functional unit having a plurality of stages [logical stages 310.1-310.N], each of said stages capable of being separately activated or deactivated based upon a respective activity indicator [enable or valid signal], where said stages of said functional unit are arranged in series [pipeline] [col.4, ll.2-5, ll.12-14].
- A stage activation controller [340 and 330 constitutes controller] that includes logic gates [330.1-330.N] that utilizes said activity indicators in conjunction with a stage activation clock pulse of a clock signal [primary clock] to determine which of said stages are to be activated or deactivated [col.4, ll.6-14, ll.27-53].

33. It would have been obvious to one of ordinary skill in the art, having the teachings of Matter and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Matter to include the teachings of Fletcher, in order to obtain the microprocessor comprising the claimed instruction evaluation unit, functional unit, and stage activation controller. One of ordinary skill in the art would have been motivated to make such a combination as it provides a refined way to decrease power consumption in a processor as the processing power increases and potential overheating is a problem [Fletcher: col.1, ll.13-32].

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34. Fletcher discloses an instruction evaluation unit [scheduler] configured to evaluate the next instruction [col.3, ll.53-67], but did not disclose explicitly that the stage activation controller is connected to it.

35. Sproch discloses a microprocessor [circuit 200a] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- A stage activation controller [propagation circuit 230] that is connected to the instruction evaluation unit [determination circuit 210] [fig.3].

36. It would have been obvious to one with ordinary skill in the art to utilize a configuration with the stage activation controller connected to the instruction evaluation unit as taught by Sproch because Applicant has not disclosed an advantage, a particular purpose, or solution to a stated problem for using said configuration. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with other less obvious configurations that would not affect the timing of the instruction and associated activity indicator processing because the Applicant's invention is intended to control the activation and deactivation of the plurality of functional stages separately, irrelevant of the explicit detailed connections of units that should obviously have been connected together because of their related task and order of executing that task.

37. As to claim 18, Bartley discloses the microprocessor that is a very long instruction word processor [col.3, ll.41-44].

38. As to claim 19, Fletcher discloses the stages have separate inputs for receiving current, the inputs capable of being separately opened or closed, the activated stages having opened inputs and the deactivated inputs having closed inputs [col.4, ll.27-60].

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39. As to claim 20, Fletcher discloses the stage activation controller is a memory unit that stores said activity indicators [col.4, ll.17-19].

40. As to claim 21, Fletcher discloses the memory unit is a register having a bit size equal to the number of stages in said functional unit, each bit location storing a respective activity indicator which indicates whether to activate or deactivate a respective stage [fig.3; col.4, ll.17-19].

41. As to claim 22, Fletcher discloses the microprocessor further comprising a plurality of functional units, each of said functional units having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator [fig.1; col.2, ll.25-34].

42. As to claim 23, Fletcher discloses the microprocessor further comprising a plurality of stage activation controllers, each of said stage activation controllers using said activity indicators to individually activate or deactivate each of said stages of a respective one of the plurality of functional units [col.4, ll.27-60].

43. As to claim 24, Fletcher discloses the microprocessor further comprising a plurality of instruction evaluation units, each of said instruction evaluation units associated with a respective one of said stage activation controllers [col.2, ll.25-34; col.3, ll.53-67].

44. As to claim 25, Fletcher discloses, wherein the logic gates [330] of the stage activation controller comprise AND type gates [fig.3].

45. Claims 26 and 28-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley in view of Fletcher and Sproch.

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46. In re claim 26, Bartley discloses a microprocessor [10] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- An instruction evaluation unit [dispatch and decode units 11b and 11c] that evaluates a next instruction to be executed and which produces activity indicators [bit level machine code of either sleep or active instructions] [col.4, ll.54-57; col.5, ll.1-2, ll.33-44, ll.51-57].
- A functional unit [L, S, M, or D] for executing instructions [col.3, ll.1-15, ll.55-61].

47. Bartley did not discuss details relating to the functional unit.

48. Fletcher discloses a microprocessor [integrated circuit] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- A functional unit [FUB logic 310] for executing instructions [col.3, ll.58-67], said functional unit having a plurality of stages [logical stages 310.1-310.N], each of said stages capable of being separately activated or deactivated based upon a respective activity indicator [enable or valid signal], where said stages of said functional unit are arranged in series [pipeline] [col.4, ll.2-5, ll.12-14].
- A stage activation controller [propagation circuit 340] that utilizes said activity indicators and causes each of said stages of said functional unit to be individually activated or deactivated [col.4, ll.27-53].
- A clock circuit [primary clock; fig.3] for supplying clock pulses to each stage of said functional unit and to said stage activation controller [col.4, ll.7-14, ll.19-23].

49. It would have been obvious to one of ordinary skill in the art, having the teachings of Bartley and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Bartley to include the functional unit as taught by Fletcher, in order

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to obtain the functional unit having the plurality of independently controlled stages. One of ordinary skill in the art would have been motivated to make such a combination as it provides a refined way to decrease power consumption in a processor as the processing power increases and potential overheating is a problem [Fletcher: col.1, ll.13-32].

50. Furthermore, Fletcher discloses a logic gate [330.1] having an input from said stage activation controller, an input from said clock circuit and an output to one of said stages of said functional unit, whereby said logic gate controls the supply of said clock pulses to said respective stage [fig.3; col.4, ll.6-14].

51. Fletcher discloses the logic gate as a NAND gate because the circuit was configured to operate as active low enabled [col.4, ll.19-21].

52. Sproch discloses a microprocessor [circuit 200a] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- An AND gate [351] having an input [371] from the stage activation controller [propagation circuit 230a], an input [240] from the clock circuit [clk; fig.5] and an output [251] to one of the stages [register 221 or stage 231], whereby said AND gate controls the supply of the clock pulses to the respective stage [col.11, ll.7-49].

53. It would have been obvious to one with ordinary skill in the art to utilize a configuration with AND gates as taught by Sproch instead of NAND gates because Applicant has not disclosed an advantage, a particular purpose, or solution to a stated problem for using AND gates. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with configurations of other logic gates because the Applicant's invention is intended to control the activation and deactivation of the plurality of functional stages separately

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according to the processing of instructions, irrelevant of the logic gates that can render the same intended results.

54. As to claim 28, Bartley discloses the microprocessor that is a very long instruction word processor [col.3, ll.41-44].

55. As to claim 29, Fletcher discloses the clock circuit has a delay circuit that causes the pulse supplied to said functional stages to be transmitted at a time slightly after the transmission of the pulse to said stage activation controller [col.4, ll.6-47].

56. As to claim 30, Fletcher discloses each of said stages have separate inputs for receiving a clock signal, the inputs capable of being separately opened or closed, the activated stages having opened inputs and the deactivated inputs having closed inputs [col.4, ll.10-14].

57. As to claim 31, Fletcher discloses the stage activation controller is a memory unit that stores said activity indicators [col.4, ll.17-19].

58. As to claim 32, Fletcher discloses the memory unit is a register having a bit size equal to the number of stages in said functional unit, each bit location storing a respective activity indicator which indicates whether to activate or deactivate a respective stage [fig.3; col.4, ll.17-19].

59. As to claim 33, Fletcher discloses the microprocessor further comprising a plurality of functional units, each of said functional units having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator [fig.1; col.2, ll.25-34].

60. As to claim 34, Fletcher discloses the microprocessor further comprising a plurality of stage activation controllers, each of said stage activation controllers using said activity indicators

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to individually activate or deactivate each of said stages of a respective one of the plurality of functional units [col.4, ll.27-60].

61. As to claim 35, Bartley discloses the microprocessor that is a very long instruction word processor [col.3, ll.41-44].

62. As to claim 36, Fletcher discloses the microprocessor further comprising a plurality of instruction evaluation units, each of said instruction evaluation units associated with a respective one of said stage activation controllers [col.2, ll.25-34; col.3, ll.53-67].

63. Claims 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matter in view of Bartley, Fletcher and Sproch.

64. In re claim 37, Matter discloses a computer system that operates in a manner that reduces power consumption [abstract], comprising:

- A microprocessor [100] wherein the microprocessor includes:
- An instruction register [cache 101] for temporarily storing a next instruction to be executed [col.5, ll.39-40; prefetches next instruction to be executed].
- An instruction evaluation unit [decoder 102 and microcode unit 103] that is connected to said instruction register such that said instruction evaluation unit receives said next instruction from said instruction register, said instruction evaluation unit being configured to evaluate said next instruction [col.5, ll.36-49].
- A functional unit [integer and floating point execution units 104 and 105] for executing instructions [col.5, ll.46-53].
- A main memory [14] for storing data, including instructions executable on microprocessor [col.5, ll.4-7].

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- At least one I/O device [signal generation device 25] [col.5, ll.26-28].
- At least one bus [11] supporting transfer of data between components of the computer system [col.4, l.67 -- col.5, l.28].

65. Matter did not discuss details of the instruction evaluation unit or the functional unit.

66. In regards to the instruction evaluation unit, Bartley discloses a microprocessor [10] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- An instruction evaluation unit [dispatch and decode units 11b and 11c] that evaluates a next instruction to be executed and which produces activity indicators [bit level machine code of either sleep or active instructions] [col.4, ll.54-57; col.5, ll.1-2, ll.33-44, ll.51-57].

67. It would have been obvious to one of ordinary skill in the art, having the teachings of Bartley and Matter, before him at the time the invention was made, to modify the microprocessor as taught by Matter to include the instruction evaluation unit as taught by Bartley, in order to obtain the microprocessor with the instruction evaluation unit for producing activity indicators. One of ordinary skill in the art would have been motivated to make such a combination as it provides a refined way to decrease power consumption in a processor [Bartley: col.2, ll.14-19].

68. In regards to the functional unit, Fletcher discloses a microprocessor [integrated circuit] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- A functional unit [FUB logic 310] for executing instructions [col.3, ll.58-67], said functional unit having a plurality of stages [logical stages 310.1-310.N], each of said stages capable of being separately activated or deactivated based upon a respective activity indicator [enable or valid signal], where said stages of said functional unit are arranged in series [pipeline] [col.4, ll.2-5, ll.12-14].

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- A stage activation controller [propagation circuit 340] that utilizes said activity indicators and causes each of said stages of said functional unit to be individually activated or deactivated [col.4, ll.27-53].

69. It would have been obvious to one of ordinary skill in the art, having the teachings of Matter and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Matter to include the functional unit as taught by Fletcher, in order to obtain the functional unit having the plurality of independently controlled stages. One of ordinary skill in the art would have been motivated to make such a combination as it provides a refined way to decrease power consumption in a processor as the processing power increases and potential overheating is a problem [Fletcher: col.1, ll.13-32].

70. Lastly, Fletcher discloses an instruction evaluation unit [scheduler] configured to evaluate the next instruction [col.3, ll.53-67], but did not disclose explicitly that the stage activation controller is connected to it.

71. Sproch discloses a microprocessor [circuit 200a] that operates in a manner that conserves power [abstract], the microprocessor comprising:

- A stage activation controller [propagation circuit 230] that is connected to the instruction evaluation unit [determination circuit 210] [fig.3].

72. It would have been obvious to one with ordinary skill in the art to utilize a configuration with the stage activation controller connected to the instruction evaluation unit as taught by Sproch because Applicant has not disclosed an advantage, a particular purpose, or solution to a stated problem for using said configuration. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with other less obvious

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configurations that would not affect the timing of the instruction and associated activity indicator processing because the Applicant's invention is intended to control the activation and deactivation of the plurality of functional stages separately, irrelevant of the explicit detailed connections of units that should obviously have been connected together because of their related task and order of executing that task.

73. As to claim 38, Bartley discloses the microprocessor that is a very long instruction word processor [col.3, ll.41-44].

74. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley and Fletcher as applied to claim 1 above, and further in view of Simonvich et al., US Patent 6308241, hereinafter Simonvich.

75. In re claim 39, Fletcher discloses the evaluation and producing steps are performed by an instruction evaluation unit [scheduler; col.3, ll.53-67]. Fletcher and Bartley did not discuss the details of an instruction register.

76. Simonvich discloses a method comprising:

- Receiving instructions at an instruction evaluation unit [instruction cache control 118] from an instruction register [cache 114; fig.1; col.3, ll.19-23].
- Receiving instructions at a functional unit [multiplexer 128 and execution 112] from the instruction register [fig.1].

77. It would have been obvious to one with ordinary skill in the art, having the teachings of Simonvich and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Fletcher to include the configuration with the instruction evaluation and functional units receiving instructions from the instruction register as taught by Simonvich,

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in order to obtain more efficient processing [Simonvich: col.2, ll.24-47]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [reduced execution cycle saves power].

Response to Arguments

78. Applicant's amendment to claims 1, 9, 17, 26, and 37 to correct the informalities objected to in the previous Office Action have been fully considered. The objection of the claims has been withdrawn.

79. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection as necessitated by amendment.

80. Applicant's arguments with respect to claims 9-16 and 39 have been fully considered but they are not persuasive. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the instant case, Examiner submits that the rejections were based on a combination of Bartley, Fletcher and Matter as discussed above. Applicant also alleges that the cited art "does not teach a shift register as claimed". Examiner disagrees as the rejection above demonstrates that Fletcher does teach a shift register [340].

81. Applicant's arguments with respect to claims 17-25 and 37 have been considered but are moot in view of the new ground(s) of rejection as necessitated by amendment.

82. Applicant's arguments with respect to claims 26 and 28-35 have been fully considered but they are not persuasive. Applicant alleges that the Bartley "teaches a decoder and dispatcher that

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get information from *fetch packets* ... don't produce or generate anything as does the claimed invention which uses the operation type to produce an activity indicator". Examiner disagrees as the rejection above demonstrates that Bartley does teach "an instruction evaluation unit that evaluates a next instruction to be executed and which produces activity indicators" [decoder gets *fetch* packets and produces *execute* packets containing active instructions that are implicit activity indicators].

83. Finally, in response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Examiner submits that all rejections, as demonstrated above, are based on knowledge found either explicitly in the cited references or within the level of ordinary skill.

Conclusion

84. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
June 5, 2005


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